PWM Controlled 180^o Analog Phase Shifter

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***Abstract*—Phase shifter is an important building block in radio frequency (RF) beamforming and multiple-input multiple-output (MIMO) systems to control the phase of the signals transmitted from the multiple antennas. This paper presents a switched-capacitor based analog phase shifter using a lattice phase equalizer, where the phase change occurs from 0^o to -180^o and the magnitude remains constant. The input signal's phase is adjusted by changing the equivalent shunt capacitances of the lattice phase equalizer by synchronously switching between two capacitors connected at the input and output sides. A pulse width modulated (PWM) signal is applied to the controlled switches connected in series with each capacitor. Thus, the phase difference is a function of the duty cycle of the PWM signal. The proposed concept is theoretically proved, the design is simulated using 65 nm CMOS technology at different frequencies, and implemented in hardware for design validation. The root mean squared error (RMSE) between the simulated and measured phase difference is 0.7^o, which is much lower than the error achieved using the other competitive methods.**

***Index Terms*—Phase shifter, PWM signal, duty cycle, lattice phase equalizer, RF beamforming.**

I. Introduction

An efficient design of fifth-generation (5G) radio hardware, phased array or multi-antenna beamforming systems, etc. requires an efficient design of RF phase shifter with minimal design complexity [1]. The energy beamforming technique is widely used to achieve efficient RF energy transfer from multiple antennas to power up the RF energy harvesting IoT nodes at the receiving end [2]. By optimally adjusting the phase of the waveforms transmitted from multiple antennas, the beam can be steered to create constructive interference at the receiving antenna and enhance the received signal strength [3]. However, the optimal design of energy transmitters with an efficient phase shifting mechanism in practical systems remains a major challenge.

The phase shifters are generally implemented using high pass or low pass or a combination of high pass and low pass filters. Based on the type of phase shifting, the phase shifters are be classified into two categories: digital phase shifters and analog phase shifters. The digital phase shifters are implemented by using switched capacitor-based method that consists of a parallel combination of capacitors each connected in series with a switch. The equivalent capacitance is varied by turning the switches ON and OFF. On the other hand, the analog phase shifters are developed using a varactor diode or MOSFET. The capacitance of the varactor diode is varied by varying the reverse bias voltage. Similarly, the gate capacitance of the MOSFET is controlled by varying the gate voltage. Depending on the active or passive components used in the design, the phase shifters are also divided into active and passive phase shifters [4].

Numerous techniques such as high-pass/low-pass networks, switched transmission lines, all-pass networks, etc. have been introduced in literature to implement phase shifters. The work in [5], proposed a 6-bit digital phase shifter in 65 nm CMOS technology to implement a full -360^o phase shift with 64 phase states. The RMS phase and magnitude errors achieved at $6 - 18$ GHz are below 1.8^o and 0.55 dB, respectively. Similarly, a frequency tunable and switched-type 5-bit digital phase shifters for mm-wave communication were proposed in [6], [7], where the measured phase error achieved within $3.6 - 8^o$. In [1], a w-band CMOS 4-bit digital phase shifter was implemented at 65 nm technology for high-power applications. The 4-bit phase shifter was implemented by optimally cascading switched-delay-type 180^o, 90^o, 45^o, and 22.5^o 1-bit phase shifters for high power and phase compression points. However, the limited number of phase states restricts achieving the required phase of the signal. The digital phase shifters also suffer a high insertion loss [8].

In contrast, the phase is varied in a continuous manner in the analog phase shifters, by varying the gate capacitance of MOSFETs. A vector modulator analog phase shifter at sub-6GHz band was proposed in [9], where a variable gain amplifier is used to control the gate capacitance to achieve the required phase. At 130 nm CMOS process, the RMS gain and phase errors achieved are respectively 1.8^o and 0.27 dB over the $0.1 - 5.7$ GHz band. A reflection-type wideband analog phase shifter employing branch line coupler circuit and varactor diode was proposed in [10] to achieve full 360^o phase shift. However, the maximum phase deviation at the band edges is 8^o. Although the analog phase shifters proposed in [4], [9], [10] provide a continuous phase, the limited range of capacitance limits the range of phase variation. Thus, Multiple phase shifters are needed to produce 360^o phase shift. Foremost, the increasing operating frequency decreases the quality factor of tuning varactors, which directly increases the phase noise [11].

To overcome the problems of analog and digital phase shifters, a new concept called hybrid phase shifter is proposed in [4], which consists of both analog and digital-type phase shifters. A continuous phase shift of up to 25.4^o is achieved using the hybrid phase shifter, which is almost twice the range of the designed analog or digital phase shifter. However, the drawbacks of digital and analog phase shifters still remain.

To this end, a simple and efficient analog phase shifter design using lattice phase equalizer is proposed in the article.

TABLE I: List of symbols

Notation	Description
V_s	Input signal amplitude
F_S	Operating frequency of the input signal
F_{sw}	Operating frequency of the PWM signal
V_{bias}	Bias voltage of PWM generator
V_{pwm}	PWM signal amplitude
D	Duty cycle of the PWM signal
L_f	Inductance of the lattice filter
C_f	Capacitance of the lattice filter
C_{f1}	Initial capacitance of phase shifter
C_{f2}	Final capacitance of phase shifter
R_0	Characteristic impedance
R_S	Input resistance
R_L	Output/load resistance
V_L	Output signal amplitude

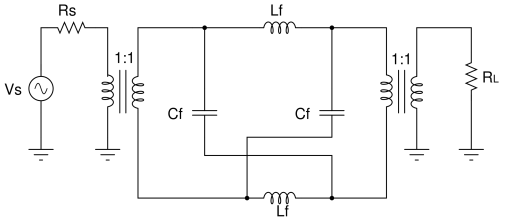


Fig. 1: Basic lattice phase equalizer circuit.

The capacitances of the lattice filter are varied using switched-capacitance based technique to adjust the phase of the signal to any value from 0^o to -180^o, while the magnitude remains constant. The capacitors are connected/disconnected to/from the circuit using controlled switches. The phase is adjusted by changing duty cycle of the PWM signal, applied at the gate of the switches connected in series with each capacitor.

The paper is organized as follows: Section II describes the proposed switched-capacitor based analog phase shifter. The simulated and experimental results are discussed in Section III, followed by the concluding remarks in Section IV.

II. Proposed Switched-Capacitor based Analog Phase Shifter

As discussed in Section I, LC filters are used to implement phase shifters such as high pass, low pass, all-pass filters, etc. The proposed design adopted a lattice filter or lattice phase equalizer to implement the phase shifter, which is a type of all-pass filter that can pass all frequency signals without changing their magnitude. The phase of the output signal varies with respect to the input signal with the variation of operating frequency and design parameters (such as inductor and capacitor values). Thus the magnitude and phase responses of the basic lattice phase equalizer, as depicted in Fig. 1, are respectively defined as $H(\omega) = 1$ and $\phi = -2\tan^{-1}(\omega\sqrt{L_f C_f})$. The lattice phase equalizer works as an all-pass filter only if $R_S = R_L = R_0$, where $R_0 = \sqrt{\frac{L}{C}}$ is the characteristic impedance of the circuit. Therefore, for a fixed frequency signal, the phase can be adjusted by changing the inductance connected in series or capacitance connected in shunt, which contributes a small variation of magnitude.

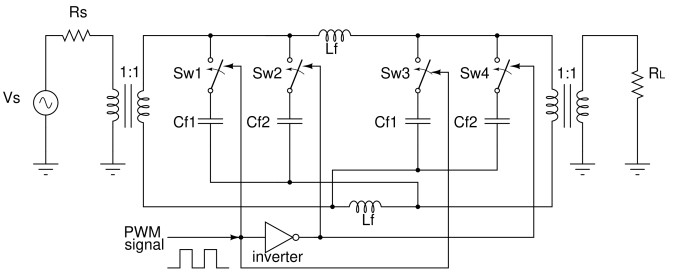


Fig. 2: Proposed PWM controlled analog phase shifter.

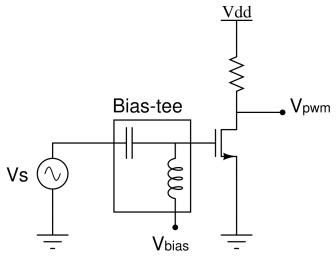


Fig. 3: PWM signal generator.

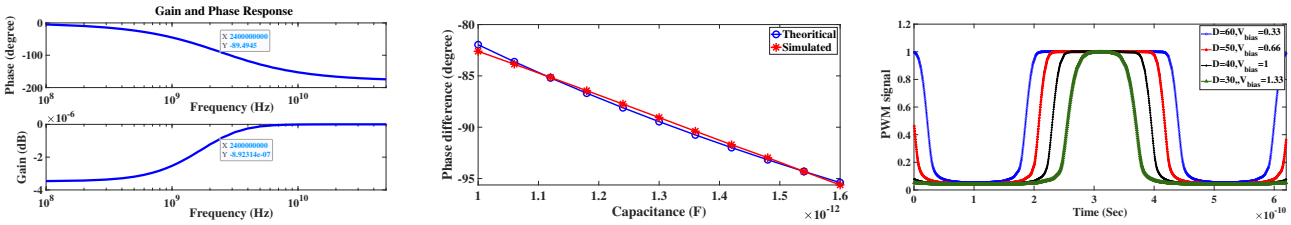
The proposed switched-capacitor based Analog Phase Shifter is shown in Fig. 2, which is implemented on a lattice phase equalizer. In this design, each of the two identical capacitors (C_f) connected in shunt at both the input and output side is split into two capacitors such that $C_f = \frac{C_{f1}+C_{f2}}{2}$. A three-terminal switch is connected in series with each capacitor to connect/disconnect the capacitor to/from the circuit. A PWM signal (V_{pwm}) is applied to the gate of the $Sw1$ and $Sw3$. And an inverted PWM signal ($\overline{V_{pwm}}$) is applied to the gate of the $Sw2$ and $Sw4$. By changing the duty cycle of the PWM signal, the equivalent capacitance of the topology can be adjusted to adapt the phase of the signal. The PWM waveform is generated from the input signal using the circuit given in Fig. 3. The V_{pwm} is applied to the switches of the proposed phase shifter. By varying the bias voltage V_{bias}, the duty cycle of the V_{pwm} is varied which finally adapts the phase of V_S. Thus, the phase difference is controlled using V_{bias}.

A. Finding Equivalent Capacitance

The values of C_f and L_f are chosen such that $\phi = 90^o$ to vary the phase from mid-point and the range is spanned from 0^o to -180^o. The range depends on C_{f1} and C_{f2}. Let, the frequency of the PWM signal is $F_{sw} = \frac{1}{T_{sw}}$ with duty cycle D, where $D = \frac{T_{ON}}{T_{sw}}$. For $0 \leq t \leq T_{ON}$, $Sw2$ and $Sw4$ are ON; only C_{f2} is connected with the circuit. For $T_{ON} \leq t \leq T_{sw}$, $Sw1$ and $Sw3$ are ON; only C_{f1} is connected with the circuit. Thus, the equivalent capacitance of the shunt connected C_{f1} and C_{f2} pair in Fig. 2 for duty cycle D is:

$$\begin{aligned} C_{eq} =& \frac{C_{f2}T_{ON} + C_{f1}T_{OFF}}{T_{ON} + T_{OFF}} \\ =& C_{f1} + D(C_{f2} - C_{f1}) \end{aligned} \tag{1}$$

where $C_{f2} \geq C_{f1}$ and $\phi = -2\tan^{-1}(\omega\sqrt{L_f C_{eq}})$. Thus, $-\phi \propto C_{eq} \propto D$.



(a) Frequency Response of lattice filter (b) variation of phase with capacitance (c) PWM signal generated at 2.4 GHz

Fig. 4: Simulation results of the conventional lattice phase equalizer and the PWM signal generator at 2.4GHz.

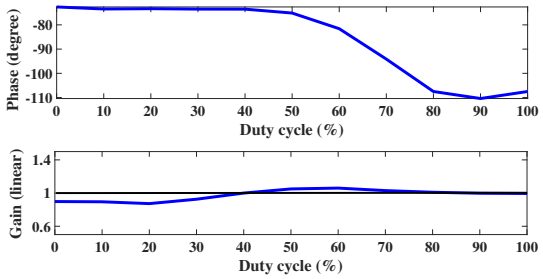


Fig. 5: variation of gain and phase with capacitance.

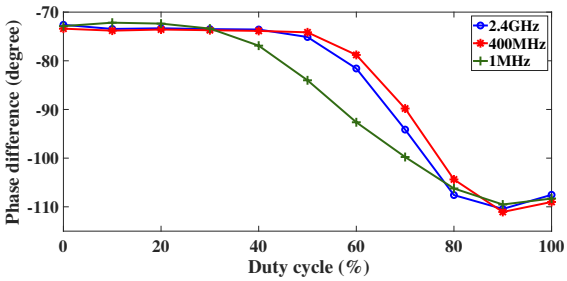


Fig. 6: Phase difference vs duty cycle at different frequencies.

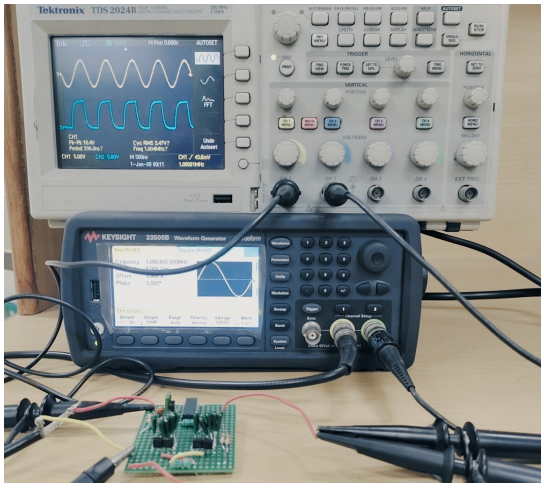


Fig. 7: Experimental setup.

III. Results and Discussion

Following the theoretical validation of the proposed design, discussed in Section II-A, the phase shifter is simulated in a 65 nm CMOS process at 2.4 GHz. To validate the simulated waveforms, the circuit is implemented in hardware at a lower frequency (e.g, 1 MHz). Section III-A and III-B describes the simulated and the experimental results, respectively.

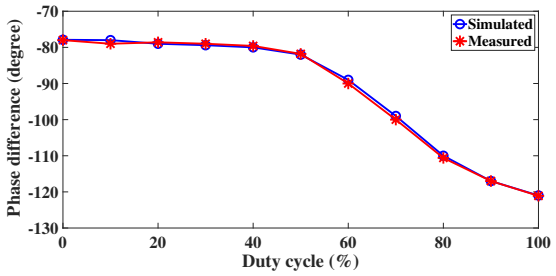
A. Simulation Results

At 2.4 GHz operating frequency, the conventional lattice phase equalizer is simulated with the specifications $\phi = 90^o$ and $R_0 = 50\ \Omega$. The computed circuit parameters are $L_f = 3.3$ nH and $C_f = 1.32$ pF. Fig. 4a shows the frequency response of the lattice phase equalizer (shown in Fig. 1). It can be observed that the phase varies from 0^o to -180^o, whereas, the gain variation is in the range of μdB. Fig. 4c shows the PWM signal generated from the circuit shown in Fig. 3 at different duty cycles. The duty cycle is adjusted by changing the bias voltage V_{bias}. The variation of phase with capacitance is shown in Fig. 4b, where the capacitances are changed directly without switching. The RMSE between theoretical and simulated phase difference, computer using (2), while changing the capacitance C_f directly is 0.32^o. However, a non-linear variation is observed across 90^o when the equivalent capacitances are changed with the switching topology, as shown in Fig. 5. The small variation of gain is also observed due to the change in the equivalent capacitance of the circuit. The RMS gain error achieved is -23.4 dB, which is much lower than the errors achieved in the competitive designs [4]. *It has been observed that the proposed method works only for* $F_{sw} = F_s$. Failing to maintain the condition, a synchronization error occurs between the input signal and PWM signal which leads to a variable phase difference at different time instants for a fixed duty cycle. However, generating PWM signal from the input signal itself ensures $F_{sw} = F_s$.

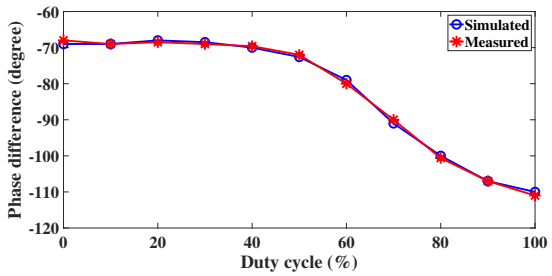
The root mean squared error between theoretical phase difference ϕ_t and simulated phase difference ϕ_s with n number of samples is defined as:

$$\text{RMSE} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(\phi_t(i) - \phi_s(i))^2}. \tag{2}$$

To analyze the frequency sensitivity of the proposed design, it is also simulated at 400 MHz and 1 MHz. For $\phi = 90^o$ and $R_0 = 50\ \Omega$, the parameters are chosen as $L_f = 20$ nH, $C_f = 7.96$ pF at 400 MHz and $L_f = 7.96\ \mu$H, $C_f = 3.18$ nF at 1 MHz. From Fig.6, it can be observed that the slope of the



(a) Phase vs duty cycle for $C_{f1} = 1$ nF and $C_{f2} = 4$ nF



(b) Phase vs duty cycle for $C_{f1} = 1.5$ nF and $C_{f2} = 5.5$ nF

Fig. 8: Comparison of simulation and experimental results of the proposed phase shifter for Fs = 1MHz.

TABLE II: Performance comparison with state-of-the-art

	Proposed phase shifter	[5]	[9]
RMS gain error	-23.4 dB	0.55 dB	0.27 dB
RMS phase error	0.7^o	1.8^o	1.8^o

phase response changes with frequency, however, the nature of graph remains similar. Thus, the proposed phase shifter works for a wide range of frequencies that covers the major RF applications.

B. Experimental Validation

The efficacy of the proposed switched-capacitor based analog phase shifter is further validated through hardware implementation. Since the circuit parasitics are more dominant than the design parameters at higher frequencies, the design accuracy decreases. Therefore, the proposed design is tested at 1 MHz. Fig. 7 shows the hardware design of the phase shifter with specifications: $V_S = 5V$, $R_0 = 50\ \Omega$, $L_f = 10\ \mu$H, $C_f = 2.5$ nF. The experiment is performed for two different ranges of capacitors. In the first experiment (exp-1), C_{f1} and C_{f2} are set as 1 nF and 4 nF to get $C_f = 2.5$ nF. Similarly, the phase variation is observed for $C_{f1} = 1.5$ nF and $C_{f2} = 5.5$ nF such that $C_f = 3.5$ nF in the second experiment (exp-2). The experimental results are shown in Fig. 8. It can be observed that the measured phase differences at different duty cycles are following the simulation results in both experiments. The RMS phase error achieved in exp-1 and exp-2 are respectively 0.7^o and 0.6^o. Performance comparison of the RMS gain and phase error of the switched-capacitor based proposed phase shifter with the state-of-the-art is listed in Table II. It shows that the proposed analog phase shifter outperforms the existing competitive designs.

IV. Concluding Remarks

A PWM controlled switched-capacitor based analog phase shifter has been proposed in this paper. The proposed phase shifter can generate continuous phase shifts of up to 180^o without changing the magnitude. Each shunt capacitor of the lattice phase equalizer has been replaced by a pair of capacitors to achieve equivalent capacitance of any value between the two capacitances. The PWM signal has been generated from the input signal of the phase shifter and the duty cycle is adjusted by varying the bias voltage of the PWM signal generator circuit. This topology makes the phase shifter more simple and more efficient compared to the state-of-the-art methods.

Acknowledgement

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